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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,413	03/12/2004	Toshiyuki Nishihara	SON-2939	6020

23353 7590 03/10/2006

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,413	NISHIHARA ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005 and 22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 16* is/are allowed.

6)☒ Claim(s) *1-4 and 10-13* is/are rejected.

7)☒ Claim(s) *5,6,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/25/05, 6/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention I, claims 1-7 and 10-16, in the reply filed on 22 December 2005 is acknowledged.

Amendment

2. Acknowledgment is made of applicant's Amendments, filed 11 April 2005 and 22 December 2005. The changes and remarks disclosed therein were considered.

Claims 8, 9 and 17-20 have been cancelled by Amendments. Therefore, claims 1-7 and 10-16 are pending in the application.

Information Disclosure Statement

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 29 June 2004 and 25 April 2005. The information disclosed therein has been considered.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

5. Claims 2, 4, 6, 10, 13 and 15 are objected to because of the following informalities:

In claim 2, lines 3, "said reading pulse" is understood as --said respective reading pulse--.

In claims 4, 6, 13 and 15, "substantially 1/2" is understood as --substantially 1/2 its level--.

In claim 10, line 4, "and applying" is understood as --and for applying-- (for further clarification).

Appropriate correction is required.

Drawings

6. Figures 16-20 should be designated by a legend such as --Prior Art-- because it appears that only that which is old is illustrated. See MPEP § 608.02(g).

Fig. 14 is objected to because G4 line is shown to be electrically connected to a drain/source of TCG, which appears to be in error.

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (U.S. Pat. No. 6,278,630).

Regarding claim 1, Yamada, for example in Figs. 15-20, discloses a data reading method in a semiconductor memory device, said semiconductor memory device having a memory cell (MC1 in Fig. 15) that stores data by state of polarization of a ferroelectric capacitor (within MC1), said data reading method comprising:

a first reading step for applying a first reading pulse (the first PL pulse in Fig. 17) to said memory cell (at PL1 in Fig. 15) to generate a first signal (through MC1, as a result of the first PL pulse and related to the first BL1 OR BL2 pulse in Fig. 17) corresponding to the stored data ("1" or "0" stored in MC1);

a writing step for writing reference signal generating data corresponding to a signal (across MC1, as a result of the middle PBLG1 pulse in Fig. 17) on a high level side to said memory cell (the PL1 side in Fig. 16 with a high level PL pulse);

a second reading step for applying a second reading pulse (the second PL pulse in Fig. 17) to said memory cell to generate a second signal (through MC1, as a result of the second PL pulse and related to the BL1 OR BL2 signal step after the first BL1 OR BL2 pulse in Fig. 17) corresponding to said reference signal generating data;

a reference signal generating step (the step of providing a different load capacitance for the second reading step by having TG2 off and TG3 on; see also Fig. 16) for generating a reference signal (on BL11) on a basis of said second signal; and

a determining step (when SA1 in Fig. 15 is enabled via SAP, SAN0 and SAP0 in Fig. 17; see also Fig. 9) for comparing said first signal with said reference signal, and determining said stored data stored in said memory cell (see also Figs. 18-20 which show another embodiment with corresponding steps as above).

Regarding claim 10, Yamada, for example in Figs. 15-20, discloses a semiconductor memory device comprising:

a memory cell (MC1 in Fig. 15) for storing data by state of polarization of a ferroelectric capacitor (within MC1);

reading means for selectively applying a reading pulse (the first or second PL pulse in Fig. 17) to said memory cell (at PL1 in Fig. 15) to generate a signal (through MC1, as a result of the first PL pulse and related to the first BL1 OR BL2 pulse in Fig. 17) corresponding to the stored data ("1" or "0" stored in MC1), and applying a first reading pulse and a second reading pulse (the two PL pulses in Fig. 17) in one reading operation to said memory cell;

writing means for, after said reading means applies the first reading pulse (the first PL pulse in Fig. 17) to the selected memory cell and a first signal (through MC1, as a result of the first PL pulse and related to the first BL1 OR BL2 pulse in Fig. 17) corresponding to the stored data of the selected memory cell is generated, writing reference signal generating data corresponding to a signal (across MC1, as a result of the middle PBLG1 pulse in Fig. 17) on a high-level side to the selected memory cell (the PL1 side in Fig. 16 with a high level PL pulse) before said reading means applies the second reading pulse;

reference signal generating means for generating a reference signal (on BL11) on a basis of a second signal (through MC1, as a result of the second PL pulse and related to the BL1 OR BL2 signal step after the first BL1 OR BL2 pulse in Fig. 17) generated by applying said second reading pulse (the second PL pulse in Fig. 17) and corresponding to said reference signal generating data stored in said selected memory cell; and

determining means (SA1 in Fig. 15) for comparing said first signal with said reference signal, and determining said stored data stored in said memory cell (see also Figs. 18-20 which show another embodiment with corresponding steps as above).

Regarding claims 3 and 12, Yamada further discloses that said semiconductor memory device further includes switch means (to control the PL pulses in Fig. 17, as applied to PL1 in Fig. 15) disposed between said memory cell (the PL1 side of MC1) and a constant-voltage node (for example, that corresponding to the high level of PL pulses); and in said writing step (or in said writing means), the reference signal generating data corresponding to the signal on the high

level side is written to said memory cell by making said switch means conduct (to generate PL pulses of Fig. 17).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Yamada (U.S. Pat. No. 6,278,630).

Regarding claims 4 and 13, Yamada discloses a method and a device as claimed in claims 1 and 10, respectively, with the exception of generating said reference signal according to said second signal by converting said second signal to substantially 1/2.

Since Yamada discloses two embodiments of providing different load capacitance when reading the reference data (Figs. 15-20), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to generate the reference signal of Yamada according to the second signal by converting the second signal to substantially 1/2 its level, since determining an optimum or workable range or an optimum value of a result effective variable (the load capacitance, and thus the signal level) requires only routine skill in the art.

11. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Yamada (U.S. Pat. No. 6,278,630) in view of Jaffe et al. (U.S. Pat. No. 5,086,412).

Regarding claims 2 and 11, Yamada discloses a method and a device as claimed in claims 1 and 10, respectively, with the exception of generating said first signal and said second signal using a remaining signal after said respective reading pulse applied is returned from a high level to a low level.

Jaffe, for example in Fig. 6, discloses generating a first signal and a second signal (determined by S1 and S2 pulses) using a remaining signal after a respective reading pulse (two DATA STROBE pulses) applied is returned from a high level to a low level (since S1 and S2 pulses occur after the DATA STROBE pulses returned to a low level).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the method and the device of Yamada, such that a remaining signal after the respective reading pulse applied returns to a low level, for the purpose of ensuring data integrity in reading the memory cell (see for example Jaffe, column 5, lines 50-52).

Allowable Subject Matter

12. Claims 7 and 16 are allowed.

Claims 5, 6, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 5 and 14, the prior arts of record do not disclose or suggest a method or a device as recited in claim 5 or 14, respectively, and particularly generating said reference

signal generated by distributing said second signal to a load having a substantially identical capacitance.

Regarding claims 6 and 15, the prior arts of record do not disclose or suggest a method or a device as recited in claim 6 or 15, respectively, and particularly generating said reference signal by short-circuiting said common node electrode and a common node electrode of an adjacent cell string and converting said second signal occurring at said common node electrode to substantially 1/2 its level.

Regarding claims 7 and 16, the prior arts of record do not disclose or suggest a method or a device as recited in claim 7 or 16, respectively, and particularly short-circuiting the gate of said current supplying transistor and the bit line, and performing a first reading from said memory cell and then disconnecting the gate of said current supplying transistor from the bit line, and performing a second reading from said memory cell.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hoffmann et al. (U.S. Pat. No. 6,317,356); Du (U.S. Pat. No. 6,459,609)

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/6/06

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh